

**Amendments to the Claims:**

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electronic device comprising:

a substrate on which an interconnect pattern is formed;

a chip component ~~having that has a base material and material, the chip component~~ having a first surface on which a pad is formed and a second surface opposite to the first surface, the chip component being mounted in such a manner that the second surface faces the substrate;

a passivation film that is formed on the first surface of the chip component, the passivation film formed to avoid at least a part of the pad,

a metal layer that is formed of a plurality of layers including a diffusion prevention layer in contact with the pad and an uppermost layer being less oxidizable than the pad, the diffusion prevention layer preventing any diffusion of material formed thereabove into the base material of the chip component;

an insulating section ~~formed above and that has a first portion disposed on the passivation film and a second portion disposed adjacent to the chip component, the insulating section being formed to come to an end at a position a distance away from the metal layer, the insulating section having a convex surface that draws a curve on a view from which a cross section perpendicular to the first surface of the chip component is taken, the convex surface ascending from the first surface to have a top surface and descending from the top surface in an outward direction, the insulating section having a portion above the first surface that has~~ first portion having a lower surface than the top surface; and

an interconnect ~~which that~~ is formed to extend from above the uppermost layer of the metal layer, ~~over the insulating section and layer~~ to above the interconnect pattern, the

interconnect having a first section disposed on the passivation film and a second section disposed over the insulating section, the interconnect covering all the lateral surfaces of the metal layer.

2. (Original) The electronic device as defined by claim 1,  
wherein the insulating section is formed of resin.

3. (Canceled)

4. (Previously Presented) The electronic device as defined by claim 1,  
further comprising a connecting layer disposed between the chip component and the substrate,  
wherein the insulating section is formed of the same material as the connecting layer.

5. (Currently Amended) A method of manufacturing an electronic device, the method comprising:

preparing a chip component and a substrate, the chip component having a base material, the chip component having a first surface on which a pad is formed and a passivation film is formed to avoid at least a part of the pad, the chip component having a second surface being opposite to the first surface, the substrate having an interconnect pattern;

mounting a~~the~~ chip component ~~having a base material and having a pad on a~~ the substrate ~~on which an interconnect pattern is formed,~~ in such a manner that ~~a~~the second surface faces the substrate, ~~the pad being formed on a first surface and the second surface being opposite to the first surface;~~ substrate;

forming a metal layer ~~of~~ that includes a plurality of layers including a diffusion prevention layer in contact with the pad and an uppermost layer being less oxidizable than the pad, the diffusion prevention layer preventing any diffusion of material formed thereabove into the base material of the chip component;

forming an insulating section ~~above and adjacent to the chip component~~ to have a convex surface that draws a curve on a view from which a cross section perpendicular to the first surface of the chip component is taken, the convex surface ascending from the first surface to have a top surface and descending from the top surface in an outward direction, the insulating section having a first portion above the first surface that has disposed on the passivation film and a second portion disposed adjacent to the chip component, the first portion having a lower surface than the top surface; ~~surface, the insulating section formed to come to an end at a position a distance away from the metal layer;~~ and

forming an interconnect in such a manner as to extend from above the uppermost layer of the metal layer, ~~over the insulating section and~~ layer to above the interconnect pattern, as to have a first section disposed on the passivation film and a second section disposed over the insulating section, and as to cover all the lateral surfaces of the metal layer.

6. (Original) The method of manufacturing an electronic device as defined by claim 5,

wherein the interconnect is formed of a dispersant including electrically conductive particles.

7. (Original) The method of manufacturing an electronic device as defined by claim 6,

wherein the step of forming the interconnect includes ejecting the dispersant including the electrically conductive particles over the metal layer, the insulating section and the interconnect pattern.

8. (Original) The method of manufacturing an electronic device as defined by claim 5,

wherein the insulating section is formed of a resin.

9. (Original) The method of manufacturing an electronic device as defined by claim 6,

wherein the insulating section is formed of a resin.

10. (Original) The method of manufacturing an electronic device as defined by claim 7,

wherein the insulating section is formed of a resin.

11. (Canceled)

12. (Previously Presented) The method of manufacturing an electronic device as defined by claim 5,

further comprising disposing a connecting layer between the chip component and the substrate,

wherein the insulating section is formed of the same material as the connecting layer.

13-16. (Canceled)

17. (Original) A circuit board on which the electronic device defined by claim 1 is mounted.

18. (Original) An electronic instrument having the electronic device defined by claim 1.

19. (New) The electronic device as defined by claim 1, a part of the passivation film on which the first section of the interconnect is disposed being between the pad and the insulating section.

20. (New) An electronic device comprising:

a substrate on which an interconnect pattern is formed;

a chip component that has a base material, the chip component having a first surface on which a pad is formed and a second surface opposite to the first surface, the chip component being mounted in such a manner that the second surface faces the substrate;

a passivation film that is formed on the first surface of the chip component, the passivation film formed to avoid at least a part of the pad;

a metal layer that is formed of a plurality of layers including a diffusion prevention layer in contact with the pad and an uppermost layer being less oxidizable than the pad, the diffusion prevention layer preventing any diffusion of material formed thereabove into the base material of the chip component;

an insulating section that has a first portion disposed on the passivation film and a second portion disposed adjacent to the chip component, the insulating section having a convex surface that draws a curve on a view from which a cross section perpendicular to the first surface of the chip component is taken, the convex surface ascending from the first surface to have a top surface and descending from the top surface in an outward direction, the first portion having a lower surface than the top surface, the insulating section having an edge disposed between the pad and a part of a periphery of the chip component on which the insulating section is disposed, the edge being closest of the insulating section to the pad; and

an interconnect that is formed to extend from above the uppermost layer of the metal layer to above the interconnect pattern, the interconnect having a first section disposed on the passivation film and a second section disposed over the insulating section, the interconnect covering all the lateral surfaces of the metal layer.